*EE/CprE/SE 492 Status Report 6*
*March 27 – April 9*

***Group number:*** **22**

***Project title:*** **ReRAM Compute ASIC Fabrication**

***Client &/Advisor:*** **Cheng Wang & Henry Duwe**

***Team Members/Role:***

**Ali Mannan**
**Tyler Kloser**
**Austin Miller**
**Vinicius Malaman Soares**

---

- **Weekly Summary**
  - Provided update to clients in weekly design meeting
  - ADC progressing with a working Vref and comparator structure with the flash ADC architecture
  - Completed precheck for the first module, inverter (last step in the process before manufacturing)
  - Nearly completed a full 1-bit design up to the schematic stage
  - Identified a new architecture to characterize and discussed with client
- **Past week accomplishments**
  - Vinicius Malaman Soares: Got the comparators on the ADC to work, started working on the logic gates for the priority encoder
  - Tyler Kloser: Successfully passed our inverter through precheck, Now have the 1T1R and opamp components in the Caravel Harness and trying precheck
  - Ali Mannan: Worked on transmission gates and proposed an alternative architecture (2T1R) to characterize. Discussed with client (Dr. Wang) and it was agreed that it would be a worthwhile characterization. Made progress into incorporating a full 1 bit design, with a schematic that simulates and works for any operations involving compute with SET functions.
  - Austin Miller: Got schematics from Jason for the previous tapeout and was able to view all devices in xschem from them, will try running LVS against it next. Started gathering/mapping our modules for placement and performing clients desired tests.
- **Pending issues**
  - Tyler Kloser: Precheck only does SKY130A tech and the ReRAM is only available using SKY130B tech
  - Ali Mannan: N/A
  - Austin Miller: Need to figure out constraints of Logic Analyzer pins and programming the management core

- Vinicius Malaman Soares:  N/A

- **Individual contributions**

| NAME | Individual Contributions | Hours this period | HOURS cumulative |
|---|---|---|---|
| Tyler Kloser | Inverter through precheck, testing opamp and 1T1R | 9 | 40 |
| Ali Mannan | Full 1 bit design works up to SET functions, with support for read and write modes. Proposed 2T1R structure. | 8 | 65 |
| Austin Miller | Brought in old schematics, mapped out testing moddules | 8 | 64 |
| Vinicius Malaman Soares | Comparators on the ADC, logic gate building | 5 | 40 |

- **Comments and extended discussion**
    - N/A

**Plans for the upcoming week**

- Ali Mannan: Progress with transmission gate to layout, characterize (in simulation) any differences observed with 2T1R structure. Progress further with a completed 1-bit schematic that also supports RESET writes and computes.
- Tyler Kloser: Perform precheck on 1T1R and op-amp components, identify a workaround (if possible) to the Sky130A and Sky130B issue with ReRAM precheck
- Austin Miller: Run LVS on with Jason's previous design and possibly create testbenches to see if we can reuse any of his components. Also, look into programming management core to run tests and obtain results on chip.
- Vinicius Malaman Soares: Finish working on the logic gates, start working on next steps

- **Summary of weekly advisor meeting**
    - Progress seems good
    - Any correspondence inside and outside the group should, within reason, be posted to the ChipForge Teams channel
    - 2T1R characterization is worthwhile, if time permits
    - Discussed pin availability and which pins we intend to use